NEXT: an Experimental Effort Towards Nanoelectronic Devices.

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(Received: 30 January 1998; accepted: 6 March 1998)

Abstract

The NEXT-project in Delft (NEXT: Nanoscale EXperiments and Technology) aims at creating artificial objects of nanometer size, contacted by macroscopic leads. The goal is to perform electronic transport measurements of those objects. At present, NEXT focusses on conducting molecules, metal quantum dots, and single-atom-wide metallic wires. Scanning Tunneling Microscopes (STMs) are used to create or manipulate those devices.

This paper presents a part of the experimental work presently going on in NEXT. It discusses the fabrication of silicon substrates with macroscopic on-chip metallization in combination with a clean and atomically flat surface. The processing employs an inorganic resist, lift-off of refractory metal, in-situ hydrogen plasma cleaning, and low-temperature anneal.

Our present research in nanofabrication places emphasis on patterning of a hydrogen-terminated silicon surface, where the well-known technology of STM-induced local hydrogen desorption is used. Transfer of the resulting pattern to create a metallic nanostructure can take place by selective nucleation of adatoms. For this technique we are investigating ultra-thin films of Ag and Co. Both metals can form epitaxial thin films at temperatures below the desorption temperature of hydrogen.

Introduction

Various technologies have been developed that can produce metallic nanostructures with feature sizes below 10 nm[1]. The interest in producing such small structures is for a large part due to the interest in electronic transport measurements on them, i.e. in their transistor-like or diode-like characteristics. The long-term relevance of electronic nanostructures is the prospect of future applications, in electronic integrated circuits or elsewhere. The short-term relevance is, for example, based on the fascinating aspects of mesoscopic physics which are expected, extending the recent research on structures between about 50 nm and several μm in size [2].

In general the Scanning Tunneling Microscope (STM) in ultra-high vacuum is a good choice for producing the highest resolution features, of more or less arbitrary geometry, on a flat surface. It has been proven possible with the STM to manipulate single atoms [3], and desorb single atoms [4].

We identify two challenges in applying the STM to electronic nanostructures: i) producing nanostructures that can in principle act as a transistor (e.g., a metallic Coulomb island with three terminals); ii) connecting the structure to macroscopic electrical contact leads.

Problem i) has been addressed in many different ways. One of the most promising, which is of interest for this paper, is the local depassivation of a hydrogen-passivated Si surface. Problem ii) has not been addressed so much (except in somewhat larger scale structures), and we will discuss our approach also in this paper.

Substrate preparation

For the experiments presented we typically use B-doped Si wafers ((100) or (111) orientation) of specific resistivity around 1 Ω-cm. For positioning and repositioning, markers are required, and for electrical measurements contact lines are required. Both can be combined in one metallization layer. This layer can be deposited in situ (see, e.g., [5]) or ex situ. For simplicity of handling, and quality and resolution of metallization, we have chosen to apply e-beam technology and the ex situ approach for this purpose.

Various metals can be used for metallization, we have obtained satisfactory initial results with W. This material has a number of favorable characteristics, such as high thermal robustness of the silicide [6] and possible cleaning of the oxide with hydrofluoric acid [7]. Organic electron-beam resist is usually problematic in combination with W liftoff, and in addition commonly results in hard-to-remove organic contamination on the substrate surface. Therefore we have chosen to develop an inorganic resist. Aspects of this process have been reported before [8, 9]. We describe the

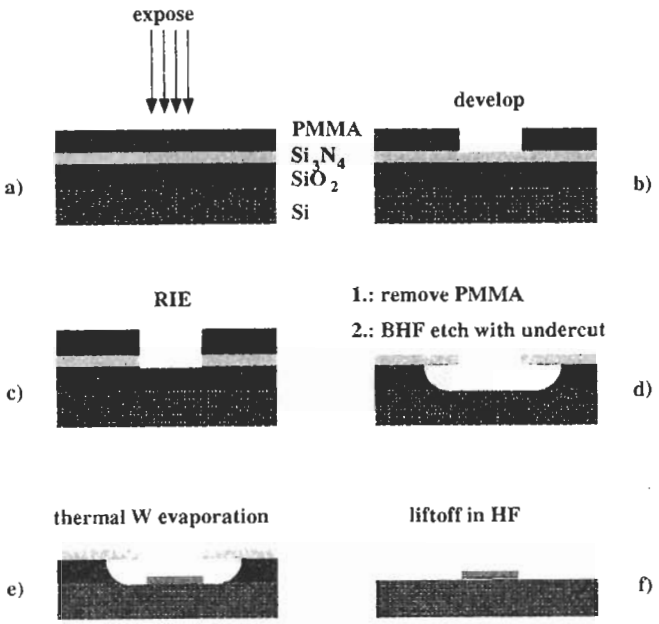

Fig.1 Inorganic resist for a liftoff process of W metallization. a) patterning of organic resist on a oxide/nitride bilayer; b) development; c) transfer in nitride by plasma etching; d) undercut in BHF; e) evaporation; and f) liftoff in HF, leaving a clean, hydrogen-terminated surface.

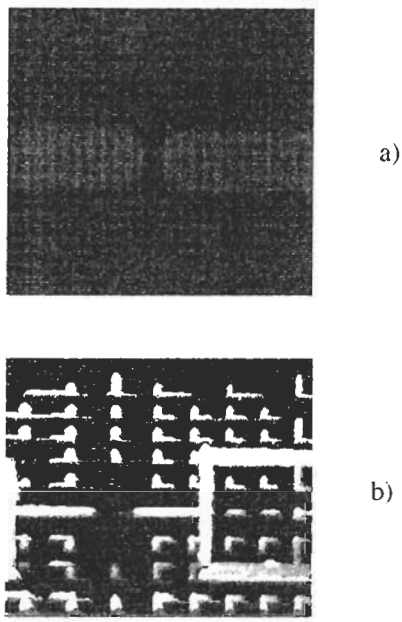

Fig.2 a)Electron micrograph of a typical contact area. The separation between the two fingers is 30 nm. The tungsten thickness is 7 nm. b) 8μm STM image of the central metallization area.

full process below.

Wafers are preferably cleaned initially, then thermally oxidized to an oxide thickness of typically 150 nm, after which low-stress nitride of 50 nm is deposited. A pattern is defined in the nitride by standard lithography and dry etching in SF_6/He plasma. The sample is then thoroughly cleaned of remaining organic resist. The pattern is transferred in the oxide by a BHF etch, after which a so-called 'undercut' profile results [10], and the Si surface is mostly hydrogen-terminated. The W is then evaporated, liftoff takes place in HF, and the sample is loaded into the experimental UHV system. Figure 1 shows the procedure in schematic. Figure 2 shows the resulting resolution after liftoff. In principle, the resolution can be as good as the available

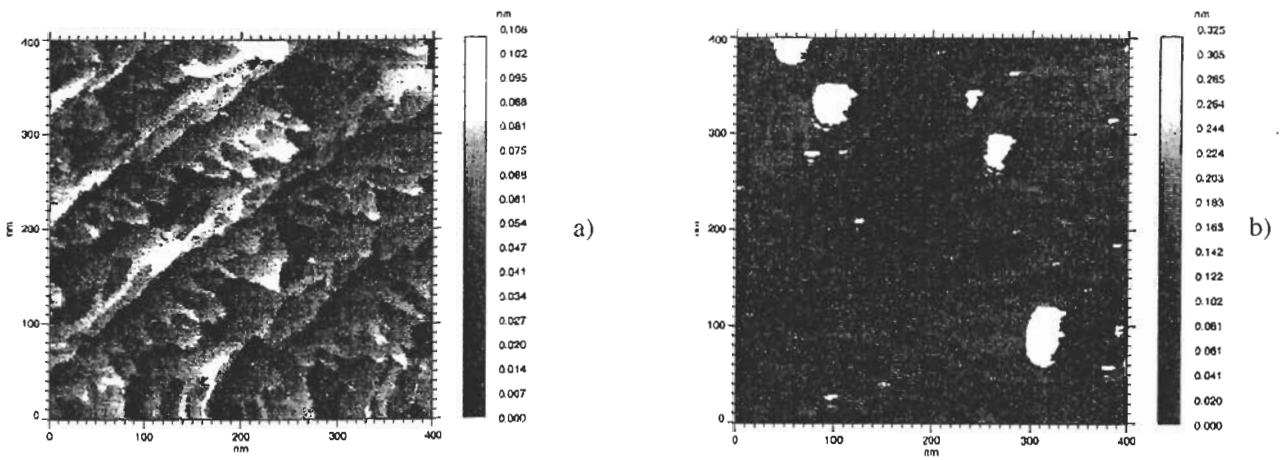

Fig.3 STM images of a Si(100) surface at 650℃ (a) and 700℃ (b).

electron-beam lithography. In this example the resolution is of order 50 nm, and the separation between the contacts is approximately 30 nm. The thickness of the W is 7 nm.

The further processing in-situ is subtle. Conventional high temperature flashing is not suitable because it breaks the continuity of the metallization. Even initial degassing at moderate temperature should be performed with caution. The Si substrate or W metallization is not protected by an oxide, and therefore a temperature treatment risks converting adsorbed hydrocarbon molecules into more problematic carbides. We follow a procedure of degassing for extended time at low temperature (450℃), i.e. below the hydrogen desorption temperature, after which the sample is further cleaned by hydrogen radical treatment. STM-inspection after this stage shows a rough surface (rms roughness of a few Å usually) which we attribute to the chemical etching by HF and hydrogen radicals. Therefore, the final step is an annealing treatment. In our variable temperature STM [11] we can follow the anneal real-time. Fig. 3 shows a sequence of anneal temperatures of an already reconstructed and atomically flat surface. It is clear that at approx. 650℃ [12] the surface atoms should be mobile enough to heal slight etch damage. At about 700℃ clusters start to appear which we think is silicon carbide. This becomes worse at higher temperature. The carbon is probably due to degassing of the STM due to the sample heating power, and/or due to remaining contamination on the sample surface.

These experiments show what the temperature window is for the final anneal step of a clean but etched substrate. Indeed, Fig. 4 shows the resulting Si surface near a metallization feature, with terraces visible. Zooming in on the terraces shows the dimer rows. It is important to note that at the anneal temperature of 750℃ the W reacts with the Si to form a silicide. This causes some trenches around the metallization, which are apparently dependent on the volume of the metallization. These trenches should be avoided in the case of device contact applications.

Finally we note that this process is still being analyzed and developed further. We are analyzing cleaning procedures with Auger and STM, and optimizing process conditions based on those results. We are also investigating

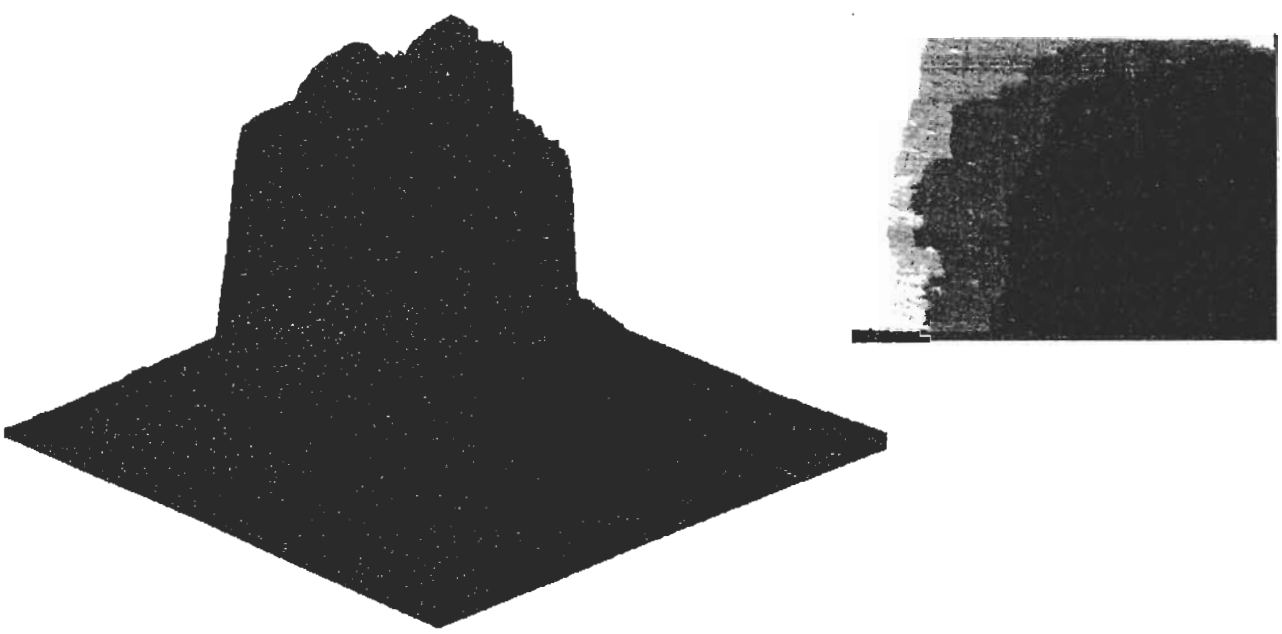

Fig.4 a) 40 nm image of tungsten silicide metallization and adjacent Si(100) terraces after the final anneal step at 750℃. The height of the metallization is approximately 20 nm. b) Higher resolution image of the terraces.

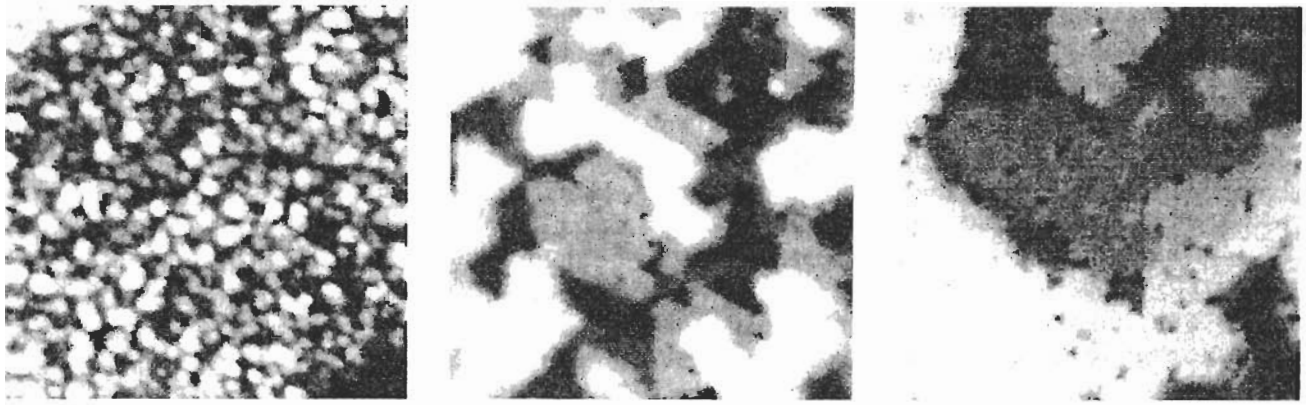

Fig.5 a) 5 Å Co film on Si(111) 7x7 after deposition at RT. b) The same film after anneal at 400℃ for 3 minutes. c) After 500℃ for 3 minutes. Image size is 50 nm. Vertical range in a) is 5 Å, in b) 12Å, and in c). 6 Å.

various other technologies, especially those which are promising for planarized contact metallization.

Thin metal films for coating of depassivated areas

As several groups have shown [5,13] it is possible to transfer a pattern defined in a hydrogen passivated silicon surface into a metallic pattern. Shen et al. [13] were able to maintain a resolution of better than 5 nm by decoration with Al adatoms. The resulting structure, however, was quite granular, which was apparently hard to avoid, and also hard to resolve by annealing.

Therefore we have studied the behaviour of other metal adatoms on bare silicon and on hydrogen passivated silicon. Since hydrogen on Si desorbs at a temperature around 480℃ [14], deposition and annealing temperatures up to this limit are relevant to be investigated.

We have studied mostly adatoms on (111) surfaces. Application of the results thus requires further development of passivation and STM lithography on this particular surface orientation. Deposition of 5 Å of Co on Si at RT results in a densely granular film with grain size of ~ 2-3 nm and grain height of a few Å (fig. 5a). This layer is thought to be composed of several bottom layers of epitaxial cobalt silicide [15] with unreacted Co on top. However, we have not yet determined the quality and domain (grain) size of this bottom epitaxial layer. Film quality improves by annealing in the relevant temperature range. Fig. 5b shows the film after a 400℃ anneal. Larger islands have formed, with steps between terraces of 1/3 and 1/6 <111> diagonal of bulk $CoSi_2$. The islands grow even further by an anneal at 500 ℃. The unexpected step heights, and further temperature treatments (up to 1200℃) will be discussed in a forthcoming publication [16].

We have also investigated diffusion lengths of Co adatoms at low density, low flux depositions on the surface of Si(100), both hydrogen passivated and bare. On bare Si the results have been discussed in the literature before [17], therefore here we will discuss some of the results of Co on passivated Si [18]. The Co evaporated onto passivated Si shows the formation of non-epitaxial islands. The density of islands shows a power law dependence on coverage, with exponent 0.29, in fair agreement with a model of an isotropic adatom random walker. Annealing at 400℃ does not significantly change the surface, but evaporation at elevated substrate temperature results in fewer but coarser islands. This is favorable for pattern transfer of depassivated areas into metal nanoelectronic structures [18].

As an alternative for Co we have also investigated Ag adatom behavior. On Si(111) 7x7, this metal forms a layer of single atom thickness of relatively high quality (large areas without defects). In combination with the abrupt interface with the Si surface (no tendency to form silicides)[19], this makes it one of the most attractive choices for pattern transfer.

We conclude that Co and Ag can be useful materials for nanolithography using pattern definition in hydrogen-passivated Si. It will be advantageous to develop techniques for high-quality hydrogen-passivation of the Si(111) surface.

Summary

In conclusion we have shown that it is feasible to produce an atomically reconstructed Si surface with metallization for electronic measurements and alignment. Such a surface is a good starting point for nanolithography using the STM. We have also performed experiments showing that Co and Ag are promising candidates for the transfer of patterns of dangling bonds in hydrogen-passivated Si surfaces into continuous (in the case of Co epitaxial) metal patterns.

Acknowledgements

This work was supported by Delft University of Technology, and by the Dutch Foundation for Fundamental Research on Matter (FOM) which is financially supported by the Dutch Science Foundation (NWO). G.P. acknowledges support from ESPRIT research project 22953, CHARGE.

We acknowledge assistance in the experiments by Ron Hoogerheide, Norbert Koster, Charles Laman, Herman Vogelaar, and Marc Zuiddam.

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